REMARKS

Applicants appreciate the thorough examination of the present application that is reflected in the lengthy and detailed Official Action. In response, Applicants have amended Independent Claim 1 and Dependent Claim 2 to provide proper antecedent basis for the sidewall of the first conductive layer pattern. In addition, Applicants have amended Dependent Claim 13 to place it in independent form and added new Independent Claim 20. Applicants have further amended Claims 1 and 3 to correct informalities noted in the Official Action.

Applicants respectfully submit that Independent Claims 1, 13 and 20 are patentable and that the remaining dependent claims are patentable at least by virtue of depending therefrom. Applicants further submit that many of the dependent claims also are separately patentable. This analysis will be presented in detail below. For the convenience of the Examiner, this analysis will be presented in the order in which the objections and rejections were raised in the Detailed Action.

The Claims Are Patentable Under 35 USC §102

Claims 1-5 and 8-11 were rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 5,352,619 to Hong (hereinafter "Hong"). However, Applicants respectfully submit that these claims are patentable over Hong for the reasons that now will be described. For the convenience of the Examiner, this analysis will be presented in the order in which the rejections were made at Pages 4-5 of the Official Action.

With regard to Claim 1, Claim 1 as amended recites in part:

> thermally oxidizing at least a portion of the integrated circuit substrate and at least a portion of the sidewall of the first conductive layer pattern to form a thermal oxide layer on at least the portion of the integrated circuit substrate and on the sidewall of the first conductive layer pattern and to form a buried doping layer from the implanted ions beneath the thermal oxide layer[.] (Emphasis added.)

Claim 1 has been amended to repeatedly clarify that the sidewall is a sidewall of the first conductive layer pattern. Since that recitation was already present in line 3 of Claim 1, this amendment is not a narrowing amendment and the full range of equivalents continues to be available.

As clearly recited in Claim 1, the sidewall of the first conductive layer pattern is thermally oxidized in order to form a thermal oxide layer on the sidewall. In sharp contrast,

as clearly shown in Figures 2 and 3 of Hong, Hong's thermal oxide layers **32** and **34** are not formed on the sidewall of the first conductive layer pattern **14**. In particular, Hong teaches:

> A second layer of silicon nitride is deposited over the substrate by LPCVD to a thickness of between about 1000 to 5000 Angstroms. The second silicon nitride layer is anisotropically etched using a conventional dry etching leaving nitride spacers **30** on the sidewalls of the layers **14**, **16** and **18**, shown in **FIG. 2**. A self-aligned thick oxide (SATO) **32** is grown by thermal oxidation over the N+ source/drain regions ...
>
> ... a wet etch is used to remove the silicon nitride spacers **30**. ... The thick gate oxide **12** under the spacers **30** is exposed when the spacers are etched away. A second wet etch ... is used to remove the silicon oxide layer **18** and the exposed portion of the thick gate oxide **12**.
>
> A thin tunnel oxide **34** is regrown in the regions where the thick oxide was removed. (Hong, Col. 3, lines 12-37.)

Thus, as clearly described in Hong, the SATO regions **32** are grown over the N+ source/drain regions and not on the sidewalls of the polysilicon layer **14**, on which nitride spacers **30** have been deposited. As further described, and more clearly shown in Figures 2 and 3, Hong's thin tunnel oxide **34** is also not on the sidewalls of the polysilicon layer **14**, since it is grown in the regions under the spacers where the thick gate oxide **12** was removed and to a thickness of less than that of the removed thick gate oxide **12**. The thin tunnel oxide **34**, therefore, does not extend beyond the thick gate oxide **12** to the sidewall of the polysilicon layer **14**.

Hong, therefore, does not teach or suggest thermally oxidizing at least a portion of the sidewall of the first conductive layer pattern to form a thermal oxide layer on the sidewall of the first conductive layer pattern. For at least these reasons, Claim 1 is not anticipated by Hong.

Claims 2-5 and 8-11 are patentable at least per the patentability of Claim 1 from which they depend.

With regard to new Independent Claim 20, Claim 20 recites in part:

> forming a second conductive layer pattern on at least a portion of the thermal oxide layer and on at least a portion of the first conductive layer pattern, wherein the second conductive layer pattern is spaced apart from the sidewall of the first conductive layer pattern. (Emphasis added.)

As clearly recited in Claim 20, the second conductive layer pattern is not in contact with the sidewall of the first conductive layer pattern.

In contrast, as clearly shown in Figure 4, Hong's second polysilicon layer **36** is not spaced apart from the sidewall of the first polysilicon layer **14**. In particular, Hong states:

> A second polysilicon layer **36** is deposited over the first polysilicon layer **14**, the tunnel oxide layers **34**, and SATO regions **32**. (Hong, Col. 3, lines 48-51.)

Thus, as described in Hong, and more clearly shown in Figure 4, Hong's second polysilicon layer **36** is not spaced apart from the first polysilicon layer **14**. Hong, therefore, does not teach or suggest forming a second conductive layer pattern spaced apart from the sidewall of the first conductive layer pattern. For at least these reasons, Claim 20 is not anticipated by Hong.

In view of the above analysis, Applicants respectfully submit that Claims 1-5, 8-11 and 20 are patentable over Hong.

The Claims Are Patentable Under 35 USC §103

Claims 6-7 and 12-13 were rejected under 35 USC §103(a) as being unpatentable over Hong. Applicants respectfully submit that claims 6-7 and 12 are patentable as depending from a patentable independent claim for the reasons that were described in the preceding section. Moreover, Claim 7 and Independent Claim 13 also are patentable under 35 USC §103(a) based on the analysis that now will be provided. For the convenience of the Examiner, this analysis will be provided in the order in which the claims were rejected at Pages 5-6 of the Detailed Action.

With regard to Claim 7, the Official Action states:

> Hong discloses the method of forming ROM including the steps of forming a capping layer 16, another layer 18 on the capping layer, a photoresist pattern layer 20 on the layer 18. However Hong doesn't disclose that the layer 18 is an organic antireflection layer or a hard mask. It would have been obvious in the art that the layer 18 which is formed of silicon oxide would have carried out the same function as the antireflection layer or a hard mask. In addition, the limitations recited in claims 6, 7, and 12 have not been alleged by applicant to be of significant importance for patentability. (Official Action, page 6, paragraph 10.)

Contrary to the assertions quoted above, potential advantages of forming an organic antireflection layer are discussed in the Specification, which states:

> when using organic reflection layers according to some embodiments of the present invention, it is possible to reduce particle generation that may result from an unstable inorganic antireflection layer such as a silicon oxynitride layer. It is also possible to reduce or prevent shorting of the gate line. This shorting phenomena may occur conventionally when a blocking layer is formed by an inorganic antireflection layer which reacts with the nitride capping layer. Subsequently, a second polysilicon layer is stacked on the blocking layer and patterned. However, when the second polysilicon

> layer is patterned with the first polysilicon layer, the first polysilicon layer may partially remain due to the effect of the blocking layer, thereby shorting out the gate. In sharp contrast, according to some embodiments of the invention, which can use an organic capping layer, this shorting can be reduced or prevented. (Specification, page 10, lines 13-24.)

Accordingly, forming an organic antireflection layer, as opposed to an inorganic antireflection layer, was not merely an obvious design choice. Claim 7 is therefore unobvious in view of Hong.

With regard to Claim 13, the Official Action states:

> Hong discloses the method of forming ROM wherein the sidewall is not formed on the sidewall of the first conductive pattern when forming the first conductive layer and thermally oxidizing the sidewall. However, Hong fails to disclose that the sidewall spacer is not present when thermally oxidizing the substrate. It would have been obvious in the art to reduce steps by thermally oxidize the substrate and the sidewall at one time as in present invention rather than perform it in two steps such as oxidizing the substrate with the spacer, removing the spacer, and then oxidizing the sidewall. (Official Action, page 6, paragraph 10.)

In this regard, Applicants submit that Hong does not, as asserted by the Official Action, teach or suggest thermally oxidizing the sidewall of the first conductive layer pattern, as discussed above with respect to Claim 1. It would, therefore, not have been obvious in view of Hong, to remove the spacers and thermally oxidize both the substrate and the sidewall of the first conductive layer pattern at one time.

Moreover, potential advantages of avoiding the use of spacers when fabricating ROM devices and of thermally oxidizing the substrate and the sidewall of the first conductive layer pattern are discussed in the Specification:

> because there is no spacer according to some embodiments of the present invention, when forming a thermal oxide layer at the peripheral part of the first conductive pattern the peripheral part of the first polysilicon layer is oxidized, and the neighboring gate insulating layer becomes thick. In some embodiments, the capping layer can be thin and there can be no spacer, so that it is possible to reduce the time for the phosphoric acid wet etching, and to reduce or minimize the amount of oxide layer that is etched during that time. Thus, according to some embodiments of the invention, it is possible to decrease the risk of conventional insulating layer breakdown that may occur between the gate line and the buried doped layer, due to a conventional thin gate insulating layer at the sidewall of the first polysilicon layer pattern. Moreover, since the risk of insulation breakdown can be reduced, there may be no need to form a thick thermal oxide layer. Thus, process time also may be reduced. Impurity diffusion during the thermal process also may be decreased, which can reduce or prevent channel punch-through. (Specification, page 9, lines 30-34 and page 10, lines 1-9.)

Accordingly, fabricating ROM devices without forming sidewall spacers on the sidewalls of the first conductive layer pattern is not an obvious design choice. Hence, the recitations of Claim 13 are not obvious in view of Hong.

CONCLUSION

Applicants again thank the Examiner for the detailed and thorough analysis. The claim amendments and analysis presented herein have overcome the rejections under 35 USC §102 and §103, so that all of the pending claims now are in condition for allowance. If the Examiner deems that further minor amendments are desirable to place the application in condition for allowance, he is encouraged to contact the undersigned so as to expedite allowance of the present application.

Respectfully submitted,

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